WHAT IS CLAIMED IS:

1. A PMOS device having a drain junction breakdown point and a maximum impact ionization point, and including:

a gate;

a body; and

a drain formed in the body, wherein at least one of the drain junction breakdown point and the maximum impact ionization point is located within at least one of the body and the drain so as to reduce any drain breakdown voltage walk-in exhibited by the device below a predetermined value.

2. The PMOS device of claim 1, wherein both the drain junction breakdown point and the maximum impact ionization point are located sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in.

3. The PMOS device of claim 2, wherein both the drain junction breakdown point and the maximum impact ionization point are located sufficiently far from the gate that any drain breakdown voltage walk-in exhibited by the device has absolute magnitude not greater than two volts.

4. The PMOS device of claim 1, wherein the PMOS device is a high voltage power transistor, the high voltage power transistor includes an extended drain region formed in the body, the extended drain region includes the drain, a deep drain implant, and a lightly doped drain implant between the deep drain implant and the gate, at least a portion of the lightly doped drain implant is located between the drain and the gate, and at least a portion of the deep drain implant is located below the drain.

5. The PMOS device of claim 4, wherein both the drain junction breakdown point and the maximum impact ionization point are located

sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in.

6. The PMOS device of claim 4, wherein both the drain junction breakdown point and the maximum impact ionization point have been located sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value, by controlling an implant dose employed to produce the lightly doped drain implant.

7. The PMOS device of claim 6, wherein the device has been manufactured in accordance with a BiCMOS process, and the implant dose is much less than 2.23×10^{12} ions/cm^2 .

8. The PMOS device of claim 7, wherein the implant dose is at least substantially equal to 1.15×10^{12} ions/cm^2.

9. The PMOS device of claim 1, wherein the drain junction breakdown point is located sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

10. The PMOS device of claim 1, wherein the maximum impact ionization point is located sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

11. A method for manufacturing an integrated circuit including at least one PMOS device having a gate, a body, a drain formed in the body, a drain junction breakdown point, and a maximum impact ionization point, said method including the step of:

(a) producing the gate, the body, and the drain such that the gate, the drain junction breakdown point, and the maximum impact ionization point have

relative positions that cause the device to exhibit no drain breakdown voltage walk-in in excess of a predetermined value.

12. The method of claim 11, wherein step (a) is performed in such a manner as to locate both the drain junction breakdown point and the maximum impact ionization point sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in.

13. The method of claim 12, wherein step (a) is performed in such a manner that any drain breakdown voltage walk-in exhibited by the device has absolute magnitude not greater than two volts.

14. The method of claim 11, wherein the PMOS device is a high voltage power transistor having an extended drain region formed in the body, the extended drain region includes the drain, a deep drain implant, and a lightly doped drain implant, said method also including the steps of:

(b) producing the deep drain implant such that at least a portion of the deep drain implant is located below the drain; and

(c) producing the lightly doped drain implant between the deep drain implant and the gate, such that at least a portion of the lightly doped drain implant is located between the drain and the gate.

15. The method of claim 14, wherein step (a) is performed in such a manner as to locate both the drain junction breakdown point and the maximum impact ionization point sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in.

16. The method of claim 14, wherein step (c) includes the step of applying an implant dose in a controlled manner, including by controlling the implant dose such that both the drain junction breakdown point and the maximum impact ionization point are located sufficiently far from the gate to

reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

17. The method of claim 16, wherein the implant dose is much less than 2.23×10^{12} ions/cm^2 .

18. The method of claim 17, wherein the implant dose is at least substantially equal to 1.15×10^{12} ions/cm^2.

19. The method of claim 11, wherein step (a) is performed in such a manner as to locate the drain junction breakdown point sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

20. The method of claim 11, wherein step (a) is performed in such a manner as to locate the maximum impact ionization point sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

21. A method for designing a PMOS device to have a gate, a body, a drain, a drain junction breakdown point within at least one of the body and the drain, and a maximum impact ionization point within at least one of the body and the drain, said method including the step of:

(a) determining relative locations of the gate, and at least one of the drain junction breakdown point and maximum impact ionization point, which cause the device to exhibit no drain breakdown voltage walk-in in excess of a predetermined value.

22. The method of claim 21, wherein step (a) is performed in such a manner as to locate both the drain junction breakdown point and the maximum impact ionization point sufficiently far from the gate that the device exhibits no significant drain breakdown voltage walk-in.

23. The method of claim 22, wherein step (a) is performed in such a manner that any drain breakdown voltage walk-in exhibited by the device has absolute magnitude not greater than two volts.

24. The method of claim 21, wherein step (a) includes the steps of:

(b) choosing a first set of design parameters for the device; and

(c) performing at least one simulation to determine simulated location of the gate of a candidate device manufactured in accordance with the first set of design parameters relative to at least one of the maximum impact ionization point and the drain junction breakdown point of the candidate device.

25. The method of claim 24, wherein step (a) also includes the steps of:

(d) determining that each of the maximum impact ionization point and the drain junction breakdown point of the candidate device has insufficient simulated distance from the gate of said candidate device to cause said candidate device to exhibit no drain breakdown voltage walk-in in excess of the predetermined value;

(e) choosing a second set of design parameters for the device; and

(f) performing at least one simulation to determine simulated location of the gate of a second candidate device manufactured in accordance with the second set of design parameters relative to at least one of the maximum impact ionization point and the drain junction breakdown point of the second candidate device.

26. The method of claim 25, wherein step (a) also includes the step of:

(g) determining that at least one of the maximum impact ionization point and the drain junction breakdown point of the second candidate device has sufficient simulated distance from the gate of said second candidate device to cause said second candidate device to exhibit no drain breakdown voltage walk-in in excess of the predetermined value.

27. The method of claim 21, wherein the PMOS device is to have an extended drain region, the extended drain region is to include the drain, a deep drain implant, and a lightly doped drain implant, at least a portion of the deep drain implant is to be located below the drain, and at least a portion of the lightly doped drain implant is to be located between the drain and the gate, wherein step (a) includes the steps of:

(b) choosing a first set of design parameters for the device, including a candidate implant dose for producing the lightly doped drain implant; and

(c) performing at least one simulation to determine simulated location of the gate of a candidate device manufactured in accordance with the first set of design parameters relative to at least one of the maximum impact ionization point and the drain junction breakdown point of the candidate device.

28. The method of claim 27, wherein step (a) also includes the steps of:

(d) determining that each of the maximum impact ionization point and the drain junction breakdown point of the candidate device has insufficient simulated distance from the gate of said candidate device to cause said candidate device to exhibit no drain breakdown voltage walk-in in excess of the predetermined value;

(e) choosing a second set of design parameters for the device, including a reduced candidate implant dose for producing the lightly doped drain implant, wherein the reduced candidate implant dose is less than the candidate implant dose; and

(f) performing at least one simulation to determine simulated location of the gate of a second candidate device manufactured in accordance with the second set of design parameters relative to at least one of the maximum impact ionization point and the drain junction breakdown point of the second candidate device.

29. The method of claim 28, wherein step (a) also includes the step of:

(g) determining that at least one of the maximum impact ionization point and the drain junction breakdown point of the second candidate device has

sufficient simulated distance from the gate of said second candidate device to cause said second candidate device to exhibit no drain breakdown voltage walk-in in excess of the predetermined value.

30. The method of claim 21, wherein step (a) is performed in such a manner as to locate the drain junction breakdown point sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.

31. The method of claim 21, wherein step (a) is performed in such a manner as to locate the maximum impact ionization point sufficiently far from the gate to reduce any drain breakdown voltage walk-in exhibited by the device below the predetermined value.